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Anodic Ta_2O_5 for CMOS compatible low voltage electrowetting-on-dielectric device fabrication

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ABSTRACT

This paper reports a CMOS compatible fabrication procedure that enables electrowetting-on-dielectric (EWOD) technology to be post-processed on foundry CMOS technology. With driving voltages less than 15 V it is believed to be the lowest reported driving voltage for any material system compatible with post-processing on completed integrated circuits wafers. The process architecture uses anodically grown tantalum pentoxide as a pinhole free high dielectric constant insulator with an overlying 16 nm layer of Teflon-AF®, which provides the hydrophobic surface for droplets manipulation. This stack provides a very robust dielectric, which maintains a sufficiently high capacitance per unit area for effective operation at a reduced voltage (15 V) which is more compatible with standard CMOS technology. The paper demonstrates that the sputtered tantalum layer used for the electrodes and the formation of the insulating dielectric can readily be integrated with both aluminium and copper interconnect used in foundry CMOS.
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1. Introduction

In recent years lab-on-a-chip and bio-MEMS systems, which can manipulate and analyse biological fluidic samples in micro- and nano-litre scales, have emerged as a solution for automating repetitive laboratory tasks [1,2]. Digital microfluidic devices based on technologies such as dielectrophoresis (DEP), electrowetting-on-dielectrics (EWOD) and surface acoustic waves (SAW) provide a potentially reconfigurable method of obtaining a bio-MEMS system [2,3], enabling different manipulations and transport routes to be programmed using the same device. Of these, EWOD technology is an attractive option that has a low power consumption making it well suited for the design and manufacture of microfluidic systems [2]. EWOD uses surface tension as a driving force, which can be controlled by applying a suitable voltage to an array of electrodes covered by a two layer dielectric.

A key parameter in EWOD technology is the driving voltage V_D. Earlier work on electrowetting arrays required driving voltages in the range 80–100 V [4]. More recently with a more judicious choice of materials, processes and dielectric thickness, the voltage required to manipulate droplets has been reduced below 15 V [4]. However, the temperatures required for the deposition of one of these dielectric layers is well in excess of 450 °C [5], making the process incompatible with CMOS post-processing. Being able to construct EWOD structures on top of CMOS technology is attractive because it facilitates large EWOD electrode array with on-chip control and sensing. This paper reports a process architecture that matches the driving voltage of [4] while requiring process temperatures considerably less than 450 °C.

2. Background

2.1. Electrowetting-on-dielectrics

The technology of the electrocapillary phenomenon that is used has been extensively described elsewhere [1], and will only be discussed briefly. For an EWOD system, the Young–Lippmann equation predicts the contact angle (defining the surface wettability as described in [1]). The change from $\theta(0)$ to $\theta(V)$ for a droplet in terms of the applied voltage V, the relative dielectric constant ε_r, the liquid–gas surface tension γ_{lg} and the thickness t of the dielectric is given by

$$\cos\theta(V) + \frac{\varepsilon_r\varepsilon_0}{2\gamma_{lg}t}V^2 = \cos\theta(0) \quad (1)$$

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Eq. (1) identifies the important role played by the dielectric covering the electrodes in determining the driving voltage V_D required to modify the contact angle by the 40° for droplet manipulation. On a Teflon-AF® surface (commonly used EWOD hydrophobic coating), this contact angle change required is from 120° to 80°, where the Eq. (1) can then be re-written as

$$V_D^2 = \frac{0.67 \times 2\gamma_{lg}t}{\varepsilon_r \varepsilon_0} \quad (2)$$

From Eq. (2), it is clear that in order to reduce the droplet driving voltage V_D, a dielectric with a high permittivity is required. This is in addition to the requirement for this layer to be totally impervious to the liquid that forms the droplet being manipulated. Failure to meet this latter criterion leads to electrolytic action at the electrode causing the device to cease functioning. Hence, a robust pinhole free dielectric with a sufficiently high breakdown voltage that also acts as barrier to the liquid is essential for any EWOD device. Finally the dielectric also has to display a hydrophobic surface, which is not typically available with materials meeting the above specifications. As a result EWOD dielectric's typically consist of two layers; the insulating dielectric discussed above which is covered by a thin hydrophobic surface layer such as Teflon-AF®.

Table 1 compares the characteristics of some of the dielectrics which have been proposed for EWOD technology.

2.2. Large EWOD arrays and multi-level metallisation

In recent years, there has been an increased number of demonstrations of bioassays executed concurrently on a digital microfluidics-based biochip [2,6]. Furthermore, it is clear that system integration and application complexity are expected to increase steadily.

One of the advantages of a digital microfluidic system based on EWOD technology is the ability to reconfigure the system. This means that the different manipulations required can be achieved on the same electrode array by simply modifying the control software. Examples of reconfigurable digital microfluidic systems based on EWOD technology and DEP technology have been reported for sample analysis that use reagent mixing [2,7–10].

Large electrode arrays have the potential to greatly increase the reconfiguration possibilities, including:

- Greater system flexibility: increases the defect tolerance of the system, allowing increased flexibility in route selection [2,6]. More functional units, such as droplet mixers, consisting of different numbers of electrodes [2,6].
- Higher sample processing throughput: more droplet samples can be processed simultaneously.
- Finer control of droplet volume: enables the system to have a higher resolution of droplet volumes.

Several examples showing defect tolerant design and spontaneous multiple droplet manipulations on electrode arrays can be found in the literature [2,6].

Obviously in a passive EWOD system, there is no internal control circuitry available, and each driving electrode in the device must be individually addressed from a contact pad via interconnect. While the interconnect for single and double rows of electrodes can be simply implemented using a single level of metallisation, the same is not the case for arrays with electrode counts of 3 × 3 or greater. The interconnects from the inner electrodes in the $M \times N$ array to the exterior control circuit must run between the electrode gaps. This approach is demonstrated in Fig. 1 which shows a single-level-metallisation micro-heater array using a passive single-level metal addressing mechanism.

In EWOD devices the interconnects are, in effect, just small electrodes and can also suffer from unwanted wetting of non-electrode areas (Fig. 2). This wetting phenomenon will potentially affect droplet manipulation, especially when many tracks are routed between electrodes as can be observed in Fig. 1. Even when the interconnect is held at ground potential, the electrode gaps may be unacceptably wide when several tracks pass between electrodes.

Hence, for EWOD arrays equal to or larger than 3 × 3 electrodes, multi-level metallisation is required to avoid parasitic effect of interconnects by burying them beneath the EWOD functional electrodes.

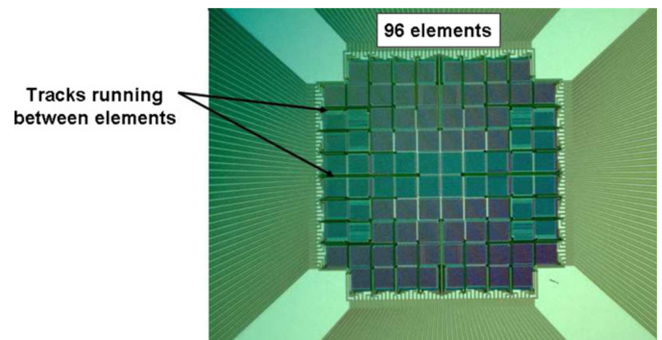

Fig. 1. Ninety six element micro-heater array, an example of a single-level-metallisation large array having interconnect tracks running between elements/electrodes.

Table 1
Comparison of EWOD dielectric properties [4,13]

	Dielectric constant	Dielectric strength (MV/cm)	Process temperature (°C)
BST	>30[a]	10	800
LPCVD SiO_2	3.8	10	900
LPCVD Si_3N_4	6–8	10	900
PECVD SiO_2	3.8	8	300
PECVD SiN_x	6–9	6	300
Parylene-C	3.1	2.7	25
Anodic Ta_2O_5	8–25[b]	6	25

[a] >100 after annealing at higher temperature.
[b] Increases with thickness (>25 when thicker than 200 nm).

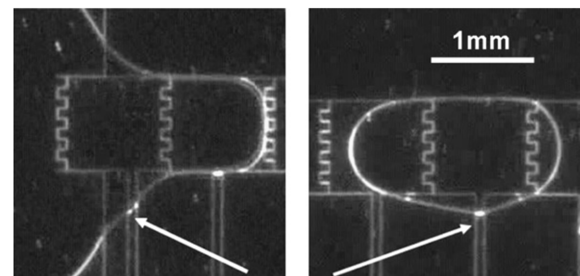

Fig. 2. Wetting phenomenon on interconnects in a single metallisation EWOD device.

2.3. Large EWOD arrays on a CMOS backplane

For arrays of EWOD electrodes, the realistic number of electrodes for passive systems is also limited by packaging considerations. For example a 30 × 30 array would require a 900 pin package which is not particulary practical.

Gong et al. partly address the packaging problem by using printed circuit board (PCB) technology together with land grid array (LGA) sockets [7]. The advantage of this solution is its low-cost and system flexibility (i.e., scalable). However, this does not solve the practical aspect of the interconnect problem entirely since a 32 × 32 digital microfluidic array used in [10] requires over 1000 pins. This is at the practical limit of a passive electrode drive system and any size bigger really requires an active controlling backplane.

CMOS technology has been widely used for row–column addressing of large numbers elements, of which the largest application is related to memory devices. Others examples include CMOS imaging chips [11] and micro displays [12]. Addressing arrays using this approach is obviously ideally suited to the realisation of EWOD arrays with a large matrix of electrodes. In addition the underlying CMOS also makes it possible to provide the electrodes with additional capabilities such as sensing (e.g., pH, temperature, light, voltage, etc) and actuation (e.g., temperature control).

Obviously a clear advantage of using on-chip addressing for large two-dimensional arrays is the significant reduction in the number of bond pads which also simplifies the packaging. A dielectrophoresis (DEP) system with a 32 × 32 array of individually addressable electrodes using a CMOS solution has already been demonstrated [10]. Manipulating droplets having more than a 100 fold volume range, it shows a scalable architecture of digital microfluidic systems based on CMOS technology [10].

In another commercialised prototype system, more than 600,000 electrodes have been embedded and separately controlled to create more than 100,000 DEP cages for droplet manipulation[1]. Similar success can be achieved with active EWOD electrode arrays (i.e. integrated CMOS backplane electrode control), if appropriate post-processing technology is available.

As part of this work an EWOD/CMOS chip has been fabricated and tested [13] (Fig. 3). This used conventional foundry processes and materials, with the EWOD post-processing involving the deposition of appropriate dielectric and surface treatment layers.

2.4. Low voltage EWOD processes

Previously reported low voltage EWOD fabrication processes have all used dielectrics deposited at high temperature (e.g., 700 °C MOCVD for barium strontium titanate [4], thermal oxidation [14], 700 °C annealed BZN (Bi_2O_3–ZnO–Nb_2O_5) [15]). None of these are compatible with CMOS technology incorporating aluminium (or copper) interconnect as deposition temperatures in excess of 450 °C are required.

In this work the CMOS foundry process that was used as the backplane of the EWOD device employed aluminium as its interconnect. Hence, the electrode metallisation and the passivation layer were determined by the foundry. For typical foundry processes the passivation is a relatively thick dielectric layer (0.5–1.0 μm) of silicon dioxide or nitride (or oxynitride), neither of which possesses a very high dielectric constant.

For an EWOD implementation using foundry passivation as the insulating dielectric a comparatively high operating voltage in the region of 70 V is required to drive droplets. This is as a direct consequence of the low dielectric constant of the passivation materials. The resulting high drive voltage requirement drove the selection of a 100 V CMOS foundry process for the demonstration EWOD backplane.

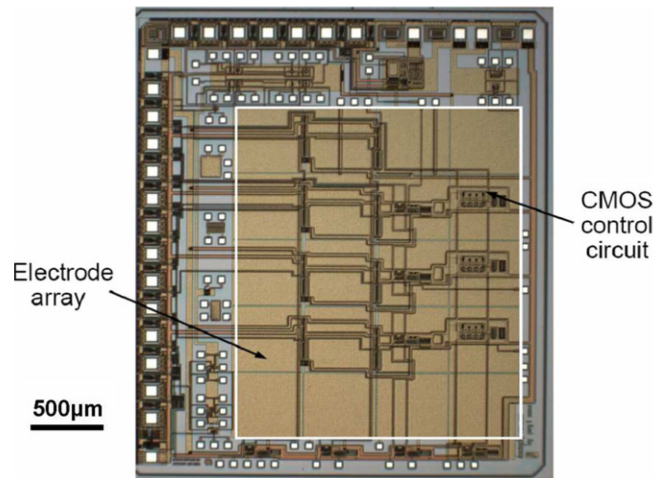

Fig. 3. EWOD electrode array (boxed area) controlled by backplane CMOS circuit [13].

Having fabricated and post-processed a high voltage CMOS EWOD device the challenge was to identify and demonstrate an improved material system that was fully compatible with EWOD, while at the same time being suitable for integration with a lower voltage CMOS technology. The material system selected is based upon a tantalum pentoxide insulating layer with a high ε_r dielectric constant (in our case around 19 at a thickness of 95 nm), which can be grown pinhole-free. This is covered by a uniform and thin (approx. 10 nm thick) overlying layer of teflon to provide the required hydrophobic surface. This material system, which involves no high temperature process (except for sputtering tantalum), simply consists of Ta/Ta_2O_5/teflon layers, which is compatible with standard foundry CMOS IC technology with aluminium interconnect.

3. Multi-level metallisation EWOD array

Multi-level metallisation EWOD arrays using chromium and chromium/platinum on glass and silicon substrates have previously been fabricated for reconfigurable multi-functional microfluidic systems [16,6].

Aluminium multilayer interconnect structures have been widely employed in standard CMOS circuitry fabrication, while a single layer of aluminium has been demonstrated as a passive EWOD electrode material in [13]. Hence, a two-level aluminium metallisation process for $M \times N$ EWOD electrode array fabrication is clearly feasible. Similar multi-level aluminium metallisation structures are commonly employed in standard CMOS integrated circuits devices.

The process flow for fabricating a two-level metallisation EWOD electrode array is detailed below and illustrated in Fig. 4:

(a) The bottom aluminium layer is sputtered on an SiO_2 insulated silicon substrate.
(b) It is then patterned to form the bond pads and the interconnects, thicknesses ranges between 0.1 and 1 μm.
(c) After patterning, 1 μm of PECVD SiO_2 is deposited as the inter-metal dielectric. Vias are then opened by patterning the PECVD SiO_2 and the second aluminium layer is then sputtered to form the electrodes an dielectrical connection to the bottom aluminium layer.

[1] <http://www/siliconbiosystems.com/DEPArray.page>.

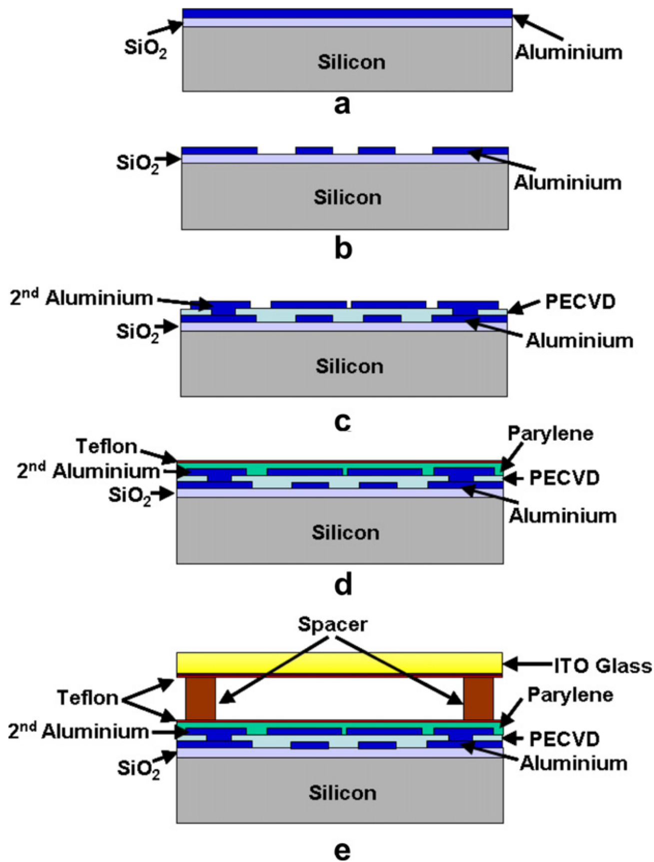

Fig. 4. Process flow for a two-level metal EWOD electrode array with aluminium as the interconnect and electrode material.

(d) After the patterning the second aluminium layer, the insulating dielectric 500 nm parylene-C (room temperature vapour deposition), and 50 nm Teflon-AF® hydrophobic layers (spin-coating) were finally deposited.
(e) After dicing the microscope slide sized chip can then be probed or packaged in the same manner as for single metal systems [13].

Using the same bond pad layout and chip size discussed in [13], a 5×8 EWOD electrode array was designed. The bottom aluminium interconnect lines were 10 μm wide. The top metal electrodes were 1 mm × 1 mm interdigited square electrodes with 100 μm wide gaps in between. The electrodes were covered with a 500 nm layer of parylene-C covered by 50 nm of Teflon-AF®. This required a driving voltage of 60 V and Fig. 5 shows droplet manipulation on a 5×8 EWOD electrode array.

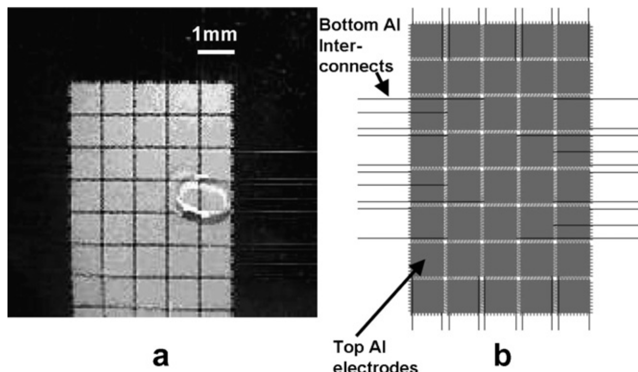

Fig. 5. (a) Photograph of a moving droplet on a two-level metallisation (aluminium) 5×8 EWOD electrode array with a driving voltage of 60 V. This is a two-plate EWOD device with a 440 μm droplet height. (b) Layout of the 5×8 EWOD electrode array.

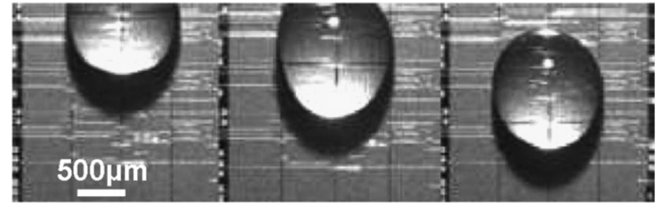

Fig. 6. Droplet movement (three frames, left to right) on a post-processed EWOD electrode array controlled by a CMOS backplane.

By using the same post-process steps on a custom designed CMOS backplane chip, droplet movement was achieved with a drive voltage of 60 V as shown in Fig. 6.

4. Tantalum–aluminium structures for low voltage EWOD–CMOS systems

As has been previously mentioned a low voltage EWOD electrode array based upon a high-K tantalum pentoxide insulating layer has been developed. This involves no high temperature process and simply consists of Ta/Ta_2O_5/Teflon-AF® or CYTOP® layers. This is compatible with standard foundry CMOS IC technology with conventional aluminium interconnect. This section will focus on the fabrication of EWOD systems based on tantalum–aluminium structures.

4.1. Structure design and fabrication

To demonstrate the Ta_2O_5–Teflon-AF® dielectric system, the top aluminium layer in Fig. 4 was replaced by sputtered tantalum which was patterned using the same mask.

There are a number of options for etching tantalum. It can be etched in fluorine-containing plasmas such as CF_4, SF_6, and CF_3Cl with CH_3F, sometimes mixed with O_2 [17,18]. The drawback is that these processes will potentially attack any underlying PECVD SiO_2 layer, which may be problematic if the tantalum etching is not uniform. By using $SiCl_4$ mixed with NF_3 plasma, Shimada et al. obtained an etch selectivity greater than 80:1 between tantalum and SiO_2 (10:1 in absence of NF_3) [19].

An alternative is XeF_2 dry etching. This is commonly used for silicon etch release in MEMS fabrication, especially post-CMOS etch release due to its high selectivity with other materials (greater than 1000:1 for silicon to SiO_2 and aluminium) [20]. XeF_2 rapidly etches tantalum and no aluminium or SiO_2 attack was observed when using a Memsstar® tool. The only potential issue is the degree of undercut, as shown in Fig. 7 with an average value of

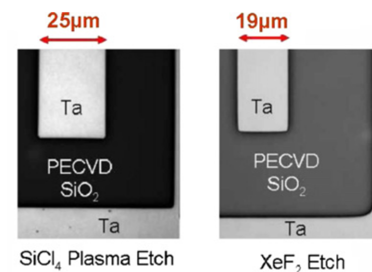

Fig. 7. Microscope photos showing a higher etching selectivity of tantalum to SiO_2 in XeF_2 gas (right) than in $SiCl_4$ plasma (left). Isotropically etched tantalum patterns in XeF_2 gas (right) have a smaller feature size than those anisotropically etched in $SiCl_4$ plasma (left).

3.0 μm on each side being measured when etching 0.45 μm thick tantalum. As the gap between EWOD electrodes in this case is 30 μm, this undercut rate is acceptable and if need be, could be accounted for by a bias in the mask.

After patterning, the tantalum electrodes are anodised with a gel form citric acid solution to form the tantalum pentoxide insulating layer [21]. In this work the applied voltage was 50 V and for the electrode array shown in Fig. 5 the current compliance was 2 mA. A thin Teflon-AF® layer is then deposited using a standard spin coater on the oxidised tantalum electrodes. The surface roughness of the anodic Ta_2O_5 has been measured using AFM to have a mean roughness R_a between 0.4 and 0.6 nm (peak-to-valley value down to few nanometers) with the Teflon-AF® layer thickness uniformity across the wafer within 10%.

The resulting two-level metal EWOD array has aluminium as the bottom metal with tantalum as the top metal electrode. The 50 V anodisation voltage used in this process resulted in 95 nm of Ta_2O_5. This was followed by a 0.3% Teflon-AF® solution (diluted in Fluorinert solvent FC-75) being spin coated at 2000 rpm for 50 s, giving 16 nm of Teflon-AF®.

4.2. Experiment and results

4.2.1. Low voltage EWOD manipulation on large arrays

A common two-plate configuration EWOD chip [22] has been used in the experiments to evaluate the Ta_2O_5/Teflon-AF® system. A conductive indium tin oxide (ITO) covered glass plate coated with 20 nm Teflon-AF® was placed above the 5 × 8 electrode array previously presented. Spacers were used to set the distance between the plates and hence the height of droplets. In this case the spacers were 258 microns. The above combination of dielectric materials on the EWOD device (95 nm Ta_2O_5 and 16 nm of Teflon-AF®) enabled deionized water to be moved with a driving voltage of 14 V (Fig. 8).

4.2.2. Droplet size manipulation using low voltage

Fig. 9 shows a digital droplet dispense system which uses a glass fibre capillary attached through a plastic ferrule as a liquid input into a two-plate EWOD system. This Ta_2O_5 low voltage EWOD system is based on a tantalum electrode array with aluminium interconnects and uses a 15 V DC drive voltage. The liquid input is pressurised through the fibre capillary from a syringe which fills up the reservoir attached to the EWOD electrodes. The liquid is then extruded and cut into droplets of by manipulating the electrodes in the EWOD array in a similar manner to that described in [22,13].

Fig. 9 shows the creation of droplets with volumes of 80 nL, 160 nL and 320 nL by switching on 1, 2 or 4 electrodes simultaneously. The volume is defined by the size of a single electrode and the gap between the two EWOD plates. In this case, each unit electrode was 1 × 1 mm in size and the gap 80 μm. More volume choices are obviously available as the electrode size reduces and the number of electrodes increases.

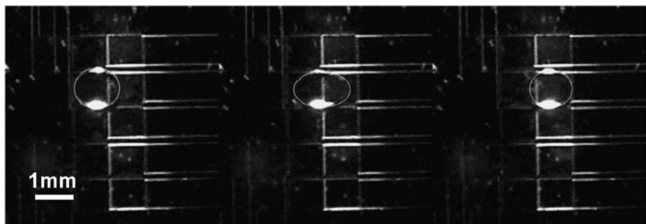

Fig. 8. Three frames (left to right) showing a moving droplet on a two-level metal EWOD chip coated with 95 nm Ta_2O_5 and 16 nm Teflon-AF® (the outlines of the droplet have been enhanced for clarity).

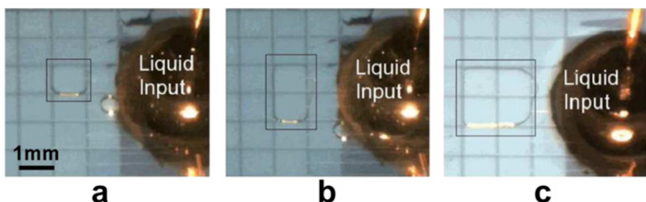

Fig. 9. Moving droplets (black boxed) with different volumes (a) 80 nL, (b) 160 nL and (c) 320 nL, dispensed from a liquid input capillary fibre (on the right of each figures).

5. Conclusion and future work

This paper has described what is believed to be the first fully CMOS compatible EWOD system that can drive liquid droplets using voltages less than 20 V. The method of producing a thin uniform film of high permittivity dielectric by the anodisation of tantalum, together with a reliable method of spinning thin uniform teflon films, are the key to achieving the required low operating potential. The resulting system, with its robust and pinhole free anodised Ta_2O_5 provides a high dielectric constant and an impervious barrier to the liquids being transported, which is not always the case with deposited dielectrics.

The integration of CMOS and EWOD technologies helps solve the issues relate to increasing the EWOD electrode array scales. The benefits have already been shown in other CMOS integrated digital microfluidic systems such as a DEP system [1] and other advantages such as possible on-chip sensing can also be obtained by integrating sensing circuits with the EWOD systems.

In addition an EWOD post-process foundry CMOS chip has been processed and droplet movement demonstrated. The next step is to significantly increase the number of electrodes so that it becomes possible to implement a programmable electrode array size and start integrating further functionality into the electrodes. Fig. 10 shows part of a prototype design that provides an example of both of these elements. It consists of an EWOD array with 200 μm × 100 μm electrodes integrated with SPADs (single photon avalanche diodes) for light detection and this gives one example of the direction digital microfluidics will be moving in the future.

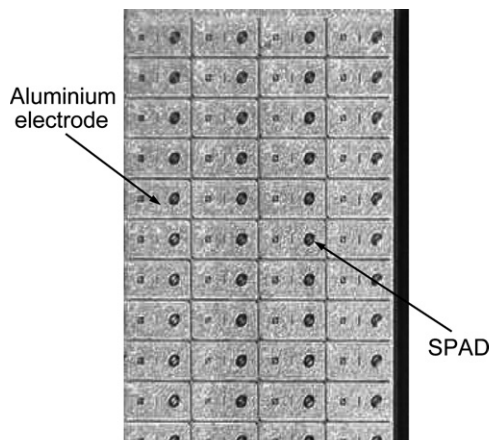

Fig. 10. A prototype design of an EWOD array with electrodes integrated with SPAD (single photon avalanche diodes) [23].

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